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Signal processing

Patent number: CN1349679
Publication date: 2002-05-15
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Classification:
- international: H03F1/32
- european:
Application number: CN20000807257 20000330
Priority number(s): GB19990007725 19990401

Also published as:
WO0060732 (A1)
EP1166433 (A1)
US6549067 (B1)
GB2348755 (A)
EP1166433 (B1)
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Abstract not available for CN1349679
Abstract of corresponding document: **US6549067**
The digital transmission sub-system comprises a DSP (100) which takes as its inputs the in-phase and quadrature channels of a baseband software radio stage. The in-phase and quadrature inputs are separately digitally predistorted (110, 120) and digitally up-converted (128) to the intermediate frequency (IF) band. The IF band signal is then converted (130) to an analogue signal which is up-converted to the radio frequency band at (134) prior to amplification at (140) to produce an RF output signal for radiation from an antenna. The predistors (110 and 120) predistort the incoming signals to counter distortion arising from the up-conversion and amplification processes within the transmission subsystem in order to linearise the RF output. The predistorters (110, 120) may be adapted using a feedback signal supplied to the DSP (100) from a splitter (142) at the output of the sub-system. The feedback mechanism may involve analogue correlation processes to permit the use of slower analogue to digital converters for providing the feedback to the DSP (100) (FIGS. 4 and 5).

Signal processing

Description of corresponding document: **US6549067**

CROSS-REFERENCE TO RELATED APPLICATION

[0002] This application claims the benefit of International Application No. PCT/GB00/01220 filed Mar. 30, 2000 and published in English, which in turn claims priority based on GB 9907725.7 filed Apr. 1, 1999.

FIELD OF THE INVENTION

[0003] This invention relates to signal processing apparatus of the kind in which an input signal is subject to both amplification and frequency conversion; and especially relates to radio telecommunications apparatus in which a voice signal is subject to amplification and frequency conversion.

BACKGROUND OF THE INVENTION

[0004] The emerging GSM-EDGE and UMTS standards for mobile telecommunications place an increasingly stringent requirement on the linearity of handsets, particularly given their proposed wider channel bandwidths. In order to realise a power-efficient handset design, some form of linearisation will be required in the handset transmitter which should be (i) low-power itself; (ii) capable of broadband linearisation (up to 5 MHz for UMTS/ULTRA; (iii) frequency flexible, and preferably multi-band; and (iv) capable of achieving and maintaining high-levels of linearity improvement with highly-non-linear power amplifiers (e.g. class-C).

[0005] According to one aspect, the invention consists in a method of linearising an output signal comprising the steps of providing an input signal, digitally predistorting the input signal using polynomial distortion generation and frequency converting it in succession to provide a predistorted, frequency-converted signal, and amplifying the predistorted, frequency-converted signal to produce an output signal.

[0006] The trend in base-station technology is toward the adoption of "software radio" techniques, i.e. architectures in which all of the modulation parameters, ramping, framing etc. take place for all channels at baseband (digitally). The combination of all channels, at appropriate frequency offsets from each other, can also be performed at baseband and the whole spectrum up-converted in a single block for multi-carrier power amplification and the transmission from a single antenna.

SUMMARY OF THE INVENTION

[0007] However, the up-conversion and power amplification need to be linear (low-distortion) in order to prevent the radiation of unwanted adjacent channel energy and hence some form of linearisation is usually required for the power amplifier. In one embodiment of the present invention, the system incorporates a digital baseband (or digital IF) interface between a baseband signal generation sub-system and a linearised transmitter sub-system performing the above method.

[0008] With the invention it is possible to allow the transmitter to become a digital-in, RF-out system with the linearisation taking place in the form of digital predistortion.

[0009] In one embodiment, the predistortion of the input signal occurs prior to its frequency conversion. Advantageously, the frequency converting step is a frequency up-conversion step.
[0010] The input signal may be provided in quadrature form comprising in-phase and quadrature channels and the predistorting step may involve predistorting each channel independently.
[0011] Advantageously, the predistortion process may involve controlling the amplitude and/or phase of some part of the predistortion. This may involve controlling the predistortion to introduce a variation of amplitude and/or phase with frequency into at least a part of the predistortion.
[0012] In one embodiment, the predistortion may be controlled on the basis of a feedback signal derived from the output signal. In such an embodiment, it is possible to inject a pilot signal into the input signal and to monitor distortion of the pilot signal in the output signal as feedback. The feedback may be used together with the generated predistortion to generate control signals controlling the predistortion. The generation of these control signals may involve the step of correlating, or mixing, predistortion with feedback. It may be advantageous to perform the step of using the predistortion together with the feedback signal to generate control signals for the predistortion at least partly in the analogue signal domain.
[0013] The predistorting process may involve generating a distortion from the input signal and reintroducing the generated distortion into the input signal. The distortion signal may be generated by mixing or multiplying the input signal with itself. The step of generating a predistortion may involve generation of different orders of distortion by mixing the input signal with itself a different number of times. Advantageously, different orders of distortion can be controlled separately.
[0014] In a preferred embodiment, the frequency conversion and predistortion processes occur within a digital signal processor.
[0015] Any of the various methods described above may be used to generate an output signal for transmission from antenna means using an input signal which has been created in the digital domain and which contains information which it is desired to transmit.
[0016] According to another aspect, the invention relates to apparatus for linearising an output signal comprising predistorting means for digitally predistorting the input signal using polynomial distortion generation and frequency converting means operating in succession on an input signal to produce a predistorted, frequency-converted signal, the apparatus further comprising amplifying means for amplifying the predistorted, frequency-converted signal to produce an output signal.

[0017] Certain embodiments of the invention will now be described, by way of example only, with reference to the figures, in which:
[0018] FIG. 1 is a diagram illustrating a digital transmission sub-system linearisation scheme;
[0019] FIG. 2 is a diagram of a predistorter;
[0020] FIG. 3 is a diagram of a non-linearity generating circuit;
[0021] FIG. 4 is a diagram illustrating a digital transmission sub-system linearisation scheme;

[0022] FIGS. 5(a-c) is a diagram illustrating a digital transmission sub-system linearisation scheme; and
[0023] FIG. 6 is a diagram illustrating a predistortion circuit.

[0024] FIG. 1 illustrates a basic digital transmitter linearisation system utilising polynomial-based predistorters. The baseband, digital input signal to the system is provided by, for example, a "software radio" architecture in which all of the modulation parameters, ramping, framing, etc. take place for all channels digitally at baseband. This input for the transmitter system of FIG. 1 is provided in the form of digital in-phase and quardrature channel inputs, I and Q respectively, which are supplied to digital signal processor (DSP) 100.
[0025] The in-phase channel input signal is digitally predistorted using in-phase channel polynomial predistorter 110, whereas the quadrature channel input signal is digitally predistorted using quadrature channel polynomial predistorter 120. The outputs from predistorters 110 and 120 are mixed, using mixers 122 and 124 respectively, into in-phase and quadrature versions respectively of a signal from local oscillator 126 by way of quadrature splitter 128. The outputs from mixers 122 and 124 are then combined digitally to produce an intermediate frequency (IF) band output signal which is converted to an analogue signal by digital to analogue converter 130. The analogue IF output signal is then bandpass filtered at 132 and, using mixer 134, is subsequently mixed with the output from local oscillator 136 to produce a signal up-converted to the radio frequency (RF) band. This RF signal is then bandpass filtered at 138 prior to being amplified by non-linear RF power amplifier 140 which provides the system output to for example, an antenna of a hand-set or base station. The purpose of the predistorters 110 and 120 in the DSP 100 is to compensate for the non-linear characteristics of the RF power amplifier (PA) 140, and possibly also of the up-conversion process, in order to linearise the response of the entire transmitter system.
[0026] The predistorters 110 and 120 function by applying a predistortion to the I and Q input channels respectively which compensates for the distortion caused by the PA 140 (and possibly also by the up-conversion process). The characteristics of the predistortions applied at 110 and 120 are controlled on the basis of a feedback signal derived from the output of PA 140 using splitter 142. The portion of the PA output fed back from this splitter is coherently downconverted by mixing it with the output of local oscillator 136 which is used to up-convert the IF signal in the main signal path. The result of this mixing process, which takes place at mixer 144, is filtered at 146 prior to being converted to a digital signal at 148 which is supplied to the DSP 100 in order to provide feedback control for the predistorters 110 and 120.
[0027] The transmitter system of FIG. 1 can be adapted in a number of ways. For example, the DSP 100 could be provided with analogue to digital converters at the in-phase and quadrature channel inputs in order to provide compatibility with an analogue baseband stage, rather than a "software radio" architecture as discussed above. Furthermore, the input to the DSP 100 could be a digital or analogue IF band input signal, which

could be quadrature downconverted digitally (after any necessary analogue to digital conversion) in the DSP prior to being processed as discussed above with reference to FIG. 1. Further modifications could also be made. For example, multi-stage upconversion from the IF to the RF band could be employed and/or an amplitude and phase polynomial model could be used in place of the in-phase and quadrature (Cartesian) model employed in FIG. 1. The up-conversion of the predistorted signal to the IF band and beyond can take place in the analogue signal domain.

[0028] FIG. 2 illustrates the form of the predistortion circuit employed for each of the predistorters 110 and 120 used in the FIG. 1 system. The in-phase or, as the case may be, quadrature channel input signal is provided to splitter 200 which distributes it to the various components of the predistorter to generate various orders of distortion (to be explained later). For example, the input signal from splitter 200 is provided to third order non-linearity generator 210 to generate a third order non-linearity which is gain and phase adjusted at 212 and 214 respectively, before being supplied to combiner 216. Any additional orders of distortion, for example, the fifth, seventh and nth, are generated and adjusted in a similar manner, and are supplied to combiner 216.

[0029] In the combiner 216, the adjusted non-linearities are recombined with the input signal to the splitter 200 which passes to the combiner 216 by way of delay element 218 which compensates the input signal for the delay experienced by the signals in the non-linearity generating paths for the various orders of distortion. Thus, the signal output from combiner 216 to mixer 122 or, as the case may be, mixer 124 comprises the sum of the predistorter input signal and the independently adjusted and generated orders of distortion.

[0030] A process by which the different orders of distortion can be generated for independent control will now be described with reference to FIG. 3. Essentially, each order of distortion is created by multiplying an input signal (i.e. the in-phase or quadrature digital input channel as supplied to the splitters 200 in predistorters 110 and 120) with itself. This process is described in detail in UK Patent Application 9804745.9. In FIG. 3, the input signal, in addition to being supplied to delay element 218 in FIG. 2, is supplied to splitter 300 which thus performs the function of splitter 200 in FIG. 2.

[0031] In the FIG. 1 embodiment, a high speed analogue to digital converter may be required to sample the IF band feedback signal. The embodiment of FIG. 4 avoids the use of resource-draining fast analogue to digital converters by using correlation processors external to the DSP as a method of simply reducing the required sampling rate of the analogue to digital converters. Only a single correlator (mixer) is shown in each of the feedback paths to the in-phase and quadrature channel predistorters (correlators 410 and 412), but the principle may be extended to a number of correlators and hence a number of orders of distortion as will be discussed later with reference to FIGS. 5a-5c. In other respects, the embodiment of FIG. 4 is similar to that of FIG. 1.

[0032] It will be apparent to the skilled person that this scheme can be extended to any desired order of distortion generation. It will also be noted

that second, fourth and sixth order distortion signals can be extracted at taps 322, 324 and 326, respectively, and these even-order distortion signals may be used in forms of predistortion control.

[0033] The operation of these correlating processes and their extension to multiple distortion orders will now be explained with reference to FIGS. 5a-5c. In the embodiment shown in these figures, the I and Q channel digital inputs are provided to digital signal processor 500 which comprises two independent predistorters 510 and 512 which operate on the I and Q channel inputs respectively. The predistorters 510 and 512 are each constituted as described with reference to FIGS. 2 and 3. An upconverter 514 frequency upconverts the I and Q predistorted signals to provide an IF band signal which is then transferred to the analogue portion of the circuit via digital to analogue converter 516. The analogue portion of the system functions in the same manner as described for the embodiment of FIG. 1 with the exception that the I and Q feedback paths terminate in splitters 518 and 520 which feed the correlation processes (described below).

[0034] An advantage of this approach to predistortion generation, is that the processing is quite simple, with each of the mixer blocks (310,312, etc) simply being equivalent to a multiplication which involves only a single instruction cycle in most DSPs. The predistortion generation mechanism operates directly on the input signals supplied at 300, and hence no memory is required to store coefficients, unlike some conventional forms of baseband predistortion generation where the memory requirement may be large, or if it is reduced, real-time interpolation calculations must be performed, thereby increasing the processing power requirement.

[0035] In the FIG. 1 embodiment, a high speed analogue to digital converter may be required to sample the IF band feedback signal. The embodiment of FIG. 4 avoids the use of resource-draining fast analogue to digital converters by using correlation processors external to the DSP as a method of simply reducing the required sampling rate of the analogue to digital converters. Only a single correlator (mixer) is shown in each of the feedback paths to the in-phase and quadrature channel predistorters (correlators 410 and 412), but the principle may be extended to a number of correlators and hence a number of orders of distortion as will be discussed later with reference to FIG. 5. In other respects, the embodiment of FIG. 4 is similar to that of FIG. 1.

[0036] This technique operates by correlating a version of the relevant baseband distortion component (for example, third order), following frequency-offset up-conversion to the IF band and digital to analogue conversion (416,418), with the downconverted (at 414) feedback signal from the amplifier output. The control signal acts to minimise this correlation result, as this will minimise the residual distortion at the output of the amplifier. The use of a small frequency offset when upconverting the distortion component ensures that the wanted IF band correlator result is at an appropriate (audio) frequency, thus removing any problems with DC offsets at the correlator output. The audio frequency result of the correlation may then be sampled by a low sample rate converter (420,422) and detected within the DSP, which eliminates the possibility of DC drifts.

[0037] It will be appreciated that although this approach uses high sampling

rate digital to analogue converters (416,418) to supply the offset baseband distortion output, this solution will, however, involve lower cost and lower power consumption than the high sampling rate analogue to digital converters which would otherwise be used in the provision of the feedback signal to the DSP in FIG. 1 embodiment (even taking into consideration the additional cost and power consumption of the low sample rate analogue to digital converters 420,422). The dynamic range (number of bits) required of the digital to analogue converters 416 and 418 will also be much smaller than that required in the analogue to digital converters of the feedback path of the FIG. 1 embodiment. This results in a further cost and power saving.

[0038] The operation of these correlating processes and their extension to multiple distortion orders will now be explained with reference to FIG. 5. In the embodiment shown in this figure, the I and Q channel digital inputs are provided to digital signal processor 500 which comprises two independent predistorters 510 and 512 which operate on the I and Q channel inputs respectively. The predistorters 510 and 512 are each constituted as described with reference to FIGS. 2 and 3. An upconverter 514 frequency upconverts the I and Q predistorted signals to provide an IF band signal which is then transferred to the analogue portion of the circuit via digital to analogue converter 516. The analogue portion of the system functions in the same manner as described for the embodiment of FIG. 1 with the exception that the I and Q feedback paths terminate in splitters 518 and 520 which feed the correlation processes (described below).

[0039] The control processing is carried out independently for the I and Q channels, thus providing independent quadrature polynomial models of the amplifier characteristic. Since the control scheme for each of the predistorters 510 and 512 is essentially the same, only that for the predistorter 512 operating on the quadrature channel digital input signal will now be described.

[0040] Each of the odd orders of distortion 522,524,526,528 generated in predistorter 512 are provided to an input of a respective mixer 530,532,534,536 to the other input of which is supplied a quadrature-shifted, offset local oscillator signal from generator 538. It will be appreciated that quadrature splitter 540 provides a corresponding in-phase version of the offset local oscillator signal to the control mechanism for predistorter 510. Returning to the control mechanism for predistorter 512, the outputs of mixers 530,532,534,536 represent the orders of distortion generated within the predistorter 512 as upconverted by the offset local oscillator signal. These signals are converted to analogue signals and are supplied to inputs of mixers 542,544,546,548. These mixers correlate the offset-upconverted distortion orders with the feedback signal provided to splitter 520.

[0041] The resulting audio range signals are sampled by a bank of analogue to digital converters and are fed to a further set of correlating mixers 550,552,554,556 within the DSP. To the other input of each of these mixers is supplied a signal derived from the correlation of the output of offset local oscillator 538 with the signal from the local oscillator 558 (in upconverter 514) at 560. The LOs 558 and 538, respectively, could have frequencies of 70 MHz and 70.001 MHz, the output of mixer 560 being at 1

KHz, the off-set frequency.

[0042] The outputs of correlators 550,552,554,556 are then integrated to supply control signals for the amplitude adjusting elements of the predistorter 512 (which were described with reference to FIG.2). Equally, the control signals produced by the integrators could be used to control the phase adjusting elements of the predistorter 512. In this way, feedback control of the predistorters 510 and 512 is achieved. Since the integration and the preceding correlation takes place digitally any possibility of DC drift or offsets degrading the level of (intermodulation) distortion is eliminated. In order for the processing to remain coherent, it is necessary for the DSP clock and the RF local oscillator(s) to be derived from the same source, or to be phase locked in some way. The simplest method of achieving this is to drive both the DSP clock and the local oscillator(s) from the same crystal reference oscillator.

[0043] It should be noted that the system could be operated in polar (amplitude and phase) format in place of the Cartesian (I & Q) format described above.

[0044] It is possible to include adaptive filtering within the predistorters to create a controlled arbitrary amplitude and/or phase versus frequency characteristic for each order of distortion generated. This can enable linearisation of an output signal which would otherwise experience unequal intermodulation distortion. As shown in FIG. 6, the basic predistortion scheme, as illustrated in FIG. 2, can be adapted by the inclusion of an adaptive filter 610, etc. in each of the paths for generating the various orders of distortion. These filters can be implemented digitally, and can be of recursive or non-recursive type, and may be adapted using a feedback signal from the output of the RF power amplifier.

[0045] The basic system may also be modified to use a pilot signal which is injected into the main signal path prior to upconversion and amplification. The pilot tone would be created within the DSP (using, for example, a numerically controlled oscillator) and added prior to upconversion of the I and Q input signals to the IF band. The pilot signal will be subject to cross-modulation distortion from the input signal proper during the upconversion and amplification processes, and this cross-modulation distortion can be fed back from the output of the RF power amplifier to control the predistorters as described in UK Patent Application 9814391.0. The cross modulation components afflicting the pilot signal can be minimised using the feedback control mechanism which, in turn, leads to minimisation of the related distortion of the main signal due to intermodulation processes.

Signal processing

Claims of corresponding document: **US6549067**

What is claimed is:

[0046] 1. A method of linearizing an output signal comprising the steps of providing an input signal, digitally predistorting the input signal using polynomial distortion generation and frequency converting it in succession to provide a predistorted, frequency-converted signal, and amplifying the predistorted, frequency-converted signal to produce an output signal, wherein the predistorting step comprises producing a predistortion from the input signal for introduction to the input signal by generating different orders of distortion from the input signal and controlling the orders of distortion independently.

[0047] 2. A method according to claim 1, wherein the predistortion of the input signal occurs prior to its frequency conversion.

[0048] 3. A method according to claim 1, wherein the frequency converting step is a frequency up-converting step.

[0049] 4. A method according to claim 1, wherein the input signal is in quadrature form comprising in-phase and quadrature channels, and the predistorting step comprises the step of predistorting each channel independently.

[0050] 5. A method according to claim 1, wherein the predistorting step comprises the step of controlling the amplitude and/or phase of the predistortion.

[0051] 6. A method according to claim 1, wherein the predistorting step comprises a step of controlling the predistortion to introduce a variation of amplitude and/or phase with frequency into the predistortion.

[0052] 7. A method according to claim 1, comprising the step of controlling the predistortion on the basis of a feedback signal derived from the output signal.

[0053] 8. A method according to claim 7, comprising the step of introducing a pilot signal into the input signal and wherein the step of controlling the predistortion on the basis of a feedback signal comprises the step of monitoring distortion of the pilot signal in the output signal.

[0054] 9. A method according to claim 7, further comprising the step of using the predistortion together with the feedback signal to generate control signals for the predistortion step.

[0055] 10. A method according to claim 9 wherein the step of using the predistortion together with the feedback signal to generate control signals comprises the step of correlating the predistortion with the feedback signal.

[0056] 11. A method according to claim 10, comprising the step of frequency converting the predistortion prior to the correlating step.

[0057] 12. A method according to claim 11, wherein the step of frequency converting the predistortion comprises the step of mixing the predistortion with a first signal at a first frequency.

[0058] 13. A method according to claim 12, wherein the step of frequency converting the input signal comprises the step of mixing it with a signal at a second frequency and the correlating step comprises the step of mixing the frequency converted predistortion with the feedback to produce intermediate signals.

[0059] 14. A method according to claim 13, wherein the correlating step comprises the step of correlating the intermediate signals with a signal whose frequency is the difference of the first and second frequencies.

[0060] 15. A method according to claim 9, wherein the step of using the predistortion together with the feedback signal to generate control signals is performed at least partly in an analogue signal domain.

[0061] 16. A method according to claim 1, wherein the predistorting step comprises, mixing or multiplying the input signal with itself to generate a distortion signal.

[0062] 17. A method according to claim 1, wherein the predistorting step comprises generating different orders of distortion by mixing the input signal with itself repeatedly.

[0063] 18. A method according to claim 1, wherein the predistortion occurs in a digital signal processor.

[0064] 19. A method according to claim 1, wherein the frequency conversion of the input signal occurs in a digital domain.

[0065] 20. A method of transmitting information wirelessly, comprising the step of manipulating the information to produce an input signal and processing the input signal by the method of any preceding claim in order to generate an output signal for transmission from antenna means.

[0066] 21. Apparatus for linearising an output signal comprising predistorting means for digitally predistorting an input signal using polynomial predistortion generation and frequency converting means operating in succession on an input signal to provide a predistorted,

frequency-converted signal, and amplifying means for amplifying the predistorted, frequency-converted signal to produce an output signal, wherein the predistorting means produces a predistortion from the input signal for introduction to the input signal by generating different orders of distortion from the input signal and controlling the orders of distortion independently.

[0067] 22. Apparatus according to claim 21, wherein the predistorting means operates on the input signal prior to the frequency converting means.

[0068] 23. Apparatus according to claim 21, wherein the frequency converting means comprises frequency up-converting means.

[0069] 24. Apparatus according to claim 21, wherein the input signal is in quadrature form comprising in-phase and quadrature channels, and the predistorting means comprises means for predistorting each channel independently.

[0070] 25. Apparatus according to claim 21, wherein the predistorting means comprises means for controlling the amplitude and/or phase of the predistortion.

[0071] 26. Apparatus according to claim 21, wherein the predistorting means comprises means for controlling the predistortion to introduce a variation of amplitude and/or phase with frequency into the predistortion.

[0072] 27. Apparatus according to claim 21, comprising control means for controlling the predistortion on the basis of a feedback signal derived from the output signal.

[0073] 28. Apparatus according to claim 27, comprising injecting means for introducing a pilot signal into the input signal and wherein the control means comprises means for monitoring distortion of the pilot signal in the output signal.

[0074] 29. Apparatus according to claim 27, further comprising control signal generating means for using the predistortion together with the feedback signal to generate control signals for the predistorting means.

[0075] 30. Apparatus according to claim 29, wherein the control signal generating means comprises correlating means for correlating the predistortion with the feedback signal.

[0076] 31. Apparatus according to claim 30, comprising predistortion frequency converting means for frequency converting the predistortion prior to its correlation by the correlating means.

[0077] 32. Apparatus according to claim 31, wherein predistortion frequency

converting means comprises predistortion mixing means for mixing the predistortion with a first signal at a first frequency.

[0078] 33. Apparatus according to claim 32, wherein the frequency converting means for frequency converting the input signal comprises means for mixing it with a signal at a second frequency and the correlating means comprises means for mixing the frequency converted predistortion with the feedback to produce intermediate signals.

[0079] 34. Apparatus according to claim 33, wherein the correlating means comprises means for correlating the intermediate signals with a signal whose frequency is the difference of the first and second frequencies.

[0080] 35. Apparatus according to claim 29, wherein the control signal generating means operates at least partly in an analogue signal domain.

[0081] 36. Apparatus according to claim 21, wherein the predistorting means comprises means for mixing or multiplying the input signal with itself to generate a distortion signal.

[0082] 37. Apparatus according to claim 21, wherein the predistorting means comprises order generating means for generating different orders of distortion by mixing the input signal with itself repeatedly.

[0083] 38. Apparatus according to claim 21, wherein the predistorting means is implemented by a digital signal processor.

[0084] 39. Apparatus according to claim 21, wherein the means for frequency converting the input signal operates in a digital domain.

[0085] 40. Apparatus for transmitting information wirelessly, comprising means for manipulating the information to produce an input signal and apparatus of claim 21 for processing the input signal in order to generate an output signal for transmission from antenna means.

[19]中华人民共和国国家知识产权局

[51]Int. Cl[7]
H03F 1/32

[12]发明专利申请公开说明书

[21]申请号 00807257.4

[43]公开日 2002年5月15日

[11]公开号 CN 1349679A

[22]申请日 2000.3.30 [21]申请号 00807257.4
[30]优先权
[32]1999.4.1 [33]GB [31]9907725.7
[86]国际申请 PCT/GB00/01220 2000.3.30
[87]国际公布 WO00/60732 英 2000.10.12
[85]进入国家阶段日期 2001.11.6
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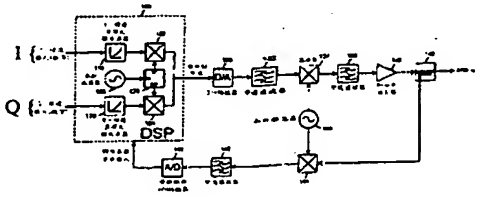
权利要求书4页 说明书7页 附图页数8页

[54]发明名称 信号处理

[57]摘要

数字发送子系统包括将基带软件无线电级的同相和正交信道作为其输入 的DSP(100)。同相和正交输入分别被数字化地预失真(110,120)并数字 化地上变频成中频(IF)频带(128)。IF 频带信号接着转换成模拟信号(130)，该模拟信号在(140)进行放大之前在(134)被上变频成射频频带,以产生 用于从天线发射的 RF 输出信号。预失真器(110 和 120)为了线性化 RF 输出，在发送子系统内预失真输入信号以抵消由上变频和放大处理产生的失真。预 失真器(110,120)可以利用从位于子系统输出的分离器(142)提供给 DSP (100)的反馈信号进行自适应调节。反馈装置可以包括模拟相关处理,以允许使用用于向 DSP(100)提供反馈的较慢的模拟－数字转换器。



ISSN1008-4274

01.11.05

权 利 要 求 书

1. 一种对输出信号进行线性化的方法，该方法包括步骤：提供输入信号；利用多项式失真生成数字化地预失真输入信号并连续地对其进行变频以提供预失真的、变频的信号；以及放大预失真的、变频的信号以产生输出信号。

2. 根据权利要求 1 所述的方法，其中输入信号的预失真在其变频之前发生。

3. 根据权利要求 1 或 2 所述的方法，其中变频步骤是上变频步骤。

4. 根据权利要求 1 至 3 中任一项所述的方法，其中输入信号采用的是包括同相和正交信道的正交形式，并且预失真步骤包括独立地对每个信道进行预失真的步骤。

5. 根据前述权利要求中任一项所述的方法，其中预失真步骤包括控制预失真的幅值和/或相位的步骤。

6. 根据前述权利要求中任一项所述的方法，其中预失真步骤包括控制预失真以将频率连同幅值和/或相位的变化引入预失真的步骤。

7. 根据前述权利要求中任一项所述的方法，包括根据从输出信号提取的反馈信号控制预失真的步骤。

8. 根据权利要求 7 所述的方法，包括将导频信号引入输入信号的步骤，并且其中根据反馈信号控制预失真的步骤包括监视输出信号中的导频信号的失真的步骤。

9. 根据权利要求 7 或 8 所述的方法，还包括利用预失真以及反馈信号以生成用于预失真步骤的控制信号的步骤。

10. 根据权利要求 9 所述的方法，其中利用预失真以及反馈信号以生成控制信号的步骤包括将预失真与反馈信号相关的步骤。

11. 根据权利要求 10 所述的方法，包括在相关步骤之前对预失真进行变频的步骤。

12. 根据权利要求 11 所述的方法，其中对预失真进行变频的步骤包括将预失真与第一频率的第一信号混合的步骤。

13. 根据权利要求 12 所述的方法，其中对输入信号进行变频的步骤包括将其与第二频率的信号混合的步骤，并且相关步骤包括将变频的预失真与反馈混合以产生中间信号的步骤。

14. 根据权利要求 13 所述的方法，其中相关步骤包括将中间信号与频率为第一和第二频率的差值的信号相关的步骤。

15. 根据权利要求 9 或 14 中任一项所述的方法，其中利用预失真以及反馈信号以生成控制信号的步骤是至少部分在模拟信号域中执行的。

16. 根据前述权利要求中任一项所述的方法，其中预失真步骤包括生成来自输入信号的失真并将所述失真重新引入输入信号。

17. 根据前述权利要求中任一项所述的方法，其中预失真步骤包括将输入信号与其本身相混合或相乘以生成失真信号。

18. 根据前述权利要求中任一项所述的方法，其中预失真步骤包括通过将输入信号与其本身重复地混合来生成不同阶的失真。

19. 根据权利要求 18 所述的方法，其中预失真步骤包括独立地控制所述阶失真的步骤。

20. 根据前述权利要求中任一项所述的方法，其中预失真在数字信号处理器中产生。

21. 根据前述权利要求中任一项所述的方法，其中输入信号的变频发生在数字域中。

22. 一种以无线方式发送信息的方法，包括为了生成用于从天线装置发送的输出信号，处理信息以产生输入信号并通过前述权利要求中任一项所述的方法来处理输入信号的步骤。

23. 如参照至少一个附图所述，一种充分地对输出信号进行线性化的方法。

24. 对输出信号进行线性化的设备，包括用于利用多项式预失真生成数字化地对输入信号进行预失真的预失真装置，和连续地在输入信号上进行运算以提供预失真的、变频的信号的变频装置，以及用于放大预失真的、变频的信号以产生输出信号的放大装置。

25. 根据权利要求 24 所述的设备，其中预失真装置在变频装置之前在输入信号上进行运算。

26. 根据权利要求 24 或 25 所述的设备，其中变频装置包括上变频装置。

27. 根据权利要求 24 至 26 中任一项所述的设备，其中输入信号采用的是包括同相和正交信道的正交形式，并且预失真装置包括独立地对每个信道进行预失真的装置。

28. 根据权利要求 24 至 27 中任一项所述的设备，其中预失真装置包括控制预失真的幅值和/或相位的装置。

29. 根据权利要求 24 至 28 中任一项所述的设备，其中预失真装置包括控制预失真以将频率连同幅值和/或相位的变化引入预失真的装置。

30. 根据权利要求 24 至 29 中任一项所述的设备，包括根据从输出信号提取的反馈信号控制预失真的控制装置。

31. 根据权利要求 30 所述的设备，包括将导频信号引入输入信号的插入装置，并且其中控制装置包括监视输出信号中的导频信号的失真的装置。

32. 根据权利要求 30 或 31 所述的设备，还包括利用预失真以及反馈信号以生成用于预失真装置的控制信号的控制信号生成装置。

33. 根据权利要求 32 所述的设备，其中控制信号生成装置包括将预失真与反馈信号相关的相关装置。

34. 根据权利要求 33 所述的设备，包括在其由相关装置进行的相关之前对预失真进行变频的预失真变频装置。

35. 根据权利要求 34 所述的设备，其中预失真变频装置包括将预失真与第一频率的第一信号混合的预失真混合装置。

36. 根据权利要求 35 所述的设备，其中对输入信号进行变频的变频装置包括将其与第二频率的信号混合的装置，并且相关装置包括将变频的预失真与反馈混合以产生中间信号的装置。

37. 根据权利要求 36 所述的设备，其中相关装置包括将中间信号与频率为第一和第二频率的差值的信号相关的装置。

38. 根据权利要求 32 至 37 中任一项所述的设备，其中控制信号生成装置是至少部分在模拟信号域中执行的。

39. 根据权利要求 24 至 38 中任一项所述的设备，其中预失真装置包括生成来自输入信号的失真并将所述失真重新引入输入信号的失真生成装置。

40. 根据权利要求 24 至 39 中任一项所述的设备，其中预失真装置包括将输入信号与其本身混合或相乘以生成失真信号的装置。

41. 根据权利要求 24 至 40 中任一项所述的设备，其中预失真装置包括通过将输入信号与其本身重复地混合来生成不同阶的失真的阶生成装置。

42. 根据权利要求 41 所述的设备，其中预失真装置包括独立地控制所述阶失真的阶控制装置。

43. 根据权利要求 24 至 42 中任一项所述的设备，其中预失真装置是由数字信号处理器实现的。

44. 根据权利要求 24 至 43 中任一项所述的设备，其中对输入信号进行变频的装置是在数字域中运行的。

45. 以无线方式发送信息的设备，包括为了生成用于从天线装置发送的输出信号，处理信息以产生输入信号并通过权利要求 24 至 43 中任一项所述的设备来处理输入信号的装置。

46. 如参照至少一个附图所述，充分地对输出信号进行线性化的设备。

说　明　书

信号处理

本发明涉及在其中对输入信号既进行放大又进行变频的类型的信号处理设备；并且更具体地说，本发明涉及对话音信号进行放大和变频的无线通信设备。

新兴的用于移动通信的 GSM-EDGE 和 UMTS 标准对手机的线性度，特别是对它们所提出的更宽信道带宽，提出了日益增加的严格的要求。为了实现节能手机的设计，会在手机发送器中要求某些形式的线性化，这类手机发送器应当是(i)本身是低功率的；(ii)能够宽带线性化（上至用于 UMTS/ULTRA 的 5MHz）；(iii)具有灵活的频率，而且最好是多频带的；以及(iv)能够利用高非线性功率放大器（例如，C 类）来完成并保持高电平线性度改进。

根据一个方面，本发明在于一种对输出信号进行线性化的方法，该方法包括步骤：提供输入信号；利用多项式失真生成（polynomial distortion generation）数字化地预失真输入信号并连续地对其进行变频以提供预失真的、变频的信号；以及放大预失真的、变频的信号以生成输出信号。

基站技术的趋势趋向于采用“软件无线电（software radio）”技术，即对所有信道的全部的调制参数、锯齿化（ramping）、分帧等在基带上出现（数字化地）的结构。在适当的相互偏移的频率上，所有信道的结合是在为多载波功率放大和来自单个天线的传输而在单个块中上变频的整个频谱和基带上执行的。

但是，为了防止所不希望的相邻信道能量的辐射，上变频和功率放大必须是线性的（低失真的），并且因此常常需要某些形式的线性化用于功率放大器。在本发明的一个实施例中，在基带信号生成子系统和执行上述方法的线性化发送器子系统之间，系统建立了数字基带（或数字 IF）接口。

利用本发明可以使发送器成为数字输入、RF 输出的系统，其中线性化以数字预失真的形式出现。

在一个实施例中，输入信号的预失真在其变频之前产生。变频步骤最好

是上变频步骤。

输入信号可以以包括同相和正交信道的正交形式提供，并且预失真步骤可以包括独立地预失真每个信道。

预失真处理最好可以包括控制预失真的某些部分的幅值和/或相位。该处理可以包括控制预失真，以将频率连同幅值和/或相位的变化引入至少预失真的一部分。

在一个实施例中，预失真可以根据从输出信号提取的反馈信号来控制。在这个实施例中，有可能将导频信号注入输入信号并监视作为反馈的输出信号中的导频信号的失真。反馈与生成的预失真一起可以用于生成控制预失真的控制信号。这些控制信号的生成可以包括相关、或混合、带有反馈的预失真的步骤。最好可以执行使用预失真以及反馈信号的步骤，以至少部分在模拟信号域中生成用于预失真的控制信号。

预失真处理可以包括从输入信号生成失真并将生成的失真重新引入输入信号。失真信号可以通过将输入信号与其本身混合或相乘来产生。产生预失真的步骤可以包括通过将输入信号与其本身相混合不同数量的次数来生成不同阶数的失真。不同阶数的失真最好能够分别被控制。

在优选实施例中，变频和预失真的处理在数字信号处理器内产生。

上述各种方法中的任一种方法，利用在数字域中产生的并包含所希望传送的信息的输入信号，可以用于产生从天线装置发送的输出信号。

根据另一方面，本发明涉及用于线性化输出信号的设备，该设备包括用于利用多项式失真生成数字化地预失真输入信号的预失真装置，和连续地在输入信号上进行运算以产生预失真的、变频的信号的变频装置，该设备还包括用于放大预失真的、变频的信号以产生输出信号的放大装置。

现在参照附图，仅以示例的方式，对本发明的某些实施例进行描述，其中：

图 1 是描述数字发送子系统线性化方法的图；

图 2 是预失真器的图；

图 3 是非线性生成电路的图；

图 4 是描述数字发送子系统线性化方法的图；

图 5 是描述数字发送子系统线性化方法的图；以及

图 6 是描述预失真电路的图。

图 1 描述了采用基于多项式的预失真器的基本数字发送器线性化系统。系统的基带、数字输入信号是由诸如“软件无线电”结构提供的，在此结构中对所有信道的全部的调制参数、锯齿化、分帧等在基带上数字化地出现。图 1 的发送器系统的输入形式是分别以数字同相和正交信道输入，I 和 Q，的形式提供的，这些输入被提供给数字信号处理器（DSP）100。

同相信道输入信号是利用同相信道多项式预失真器 110 来数字化地预失真的，而正交信道输入信号是利用正交信道多项式预失真器 120 来数字化地预失真的。利用混合器 122 和 124，采用正交分离器 128 的方式，将来自预失真器 110 和 120 的输出分别混入分别来自本地振荡器 126 的同相和正交形式（version）的信号。来自混合器 122 和 124 的输出然后数字化地结合以生成中频（IF）频带输出信号，该信号由数字－模拟转换器 130 转换成模拟信号。模拟 IF 输出信号接着在 132 进行带通滤波，并且随后利用混合器 134，与来自本地振荡器 136 的输出进行混合以生成上变频成射频（RF）频带的信号。此 RF 信号然后在被非线性 RF 功率放大器 140 放大之前在 138 进行带通滤波，放大器 140 将系统输出提供给，例如手机或者基站的天线。在 DSP 100 中的预失真器 110 和 120 的目的是为了线性化整个发送器系统的响应，补偿 RF 功率放大器（PA）140 的非线性特性，并且还可能补偿上变频处理的非线性特性。

预失真器 110 和 120 通过将预失真分别施加于 I 和 Q 输入信道来工作的，此预失真用于补偿由 PA 140（而且还可能由上变频处理）引起的失真。在 110 和 120 施加的预失真的特性是根据利用分离器 142 从 PA 140 的输出中提取的反馈信号来控制的。从该分离器反馈的部分 PA 输出通过将其与本地振荡器 136 的输出混合被相应地下变频，其中本地振荡器 136 用于在主信号路径中上变频 IF 信号。发生在混合器 144 的该混合处理的结果在 148 被转换成数字信号之前在 146 进行滤波，此数字信号是为了向预失真器 110 和 120 提供反馈控制而提供给 DSP 100 的。

图 1 的发送器系统能够以许多方式被应用。例如，为了提供与模拟基带级（stage）而不是与上述的“软件无线电”结构的兼容性，DSP 100 可以在同相和正交信道的输入上配备有模拟－数字转换器。而且，到 DSP 100 的输

入可以是数字或模拟的 IF 频带输入信号，该信号可以在按照参照图 1 的上述描述对其进行处理之前在 DSP 中被数字化地正交下变频（在任何必要的模拟－数字转换之后）。而且还能够进行修改。例如，能够采用从 IF 到 RF 频带的多级上变频，并/或能够使用幅值和相位多项式模型以替换在图 1 中使用的同相和正交（笛卡尔）模型。预失真的信号上变频成 IF 频带及更高频带能够发生在模拟信号域中。

图 2 描述了图 1 系统中预失真器 110 和 120 中的每一个所采用的预失真电路的形式。同相的或者，正如该例所示，正交信道的输入信号提供给分离器 200，分离器 200 将其分配给预失真器的各个分量以产生不同阶数的失真（后面将会解释）。例如，来自分离器 200 的输入信号在提供给组合器 216 之前，提供给第三阶非线性发生器 210 以生成分别在 212 和 214 进行增益和相位调整的第三阶非线性。任何附加阶数的失真，例如第五阶、第七阶和第 n 阶，以类似的方式被产生和调整，并提供给组合器 216。

在组合器 216 中，调整过的非线性与到分离器 200 的并经过延迟元件 218 传递到组合器 216 的输入信号重新组合，延迟元件 218 对输入信号进行补偿由生成不同阶数失真的路径的非线性中的信号所经历的延迟。因此，从组合器 216 输出到混合器 122 的，或者本例情况输出到混合器 124 中的信号包括预失真器输入信号与单独调整和生成的各阶失真的和。

现在将参照图 3 说明产生用于单独控制的不同阶失真的处理。基本上，每阶的失真是通过将输入信号（即，输入到预失真器 110 和 120 中的分离器 200 的同相或正交数字输入信道）与其自身相乘来产生的。此处理在 UK 专利申请 9804745.9 中有详细的说明。在图 3 中，输入信号除了提供给图 2 中的延迟元件 218 之外，还提供给执行图 2 中的分离器 200 的功能的分离器 300。

很显然，混合器 310 用于对输入信号求平方并且第三阶的失真信号是通过将混合器 310 的输出与混合器 312 的输入信号相混合（相乘）产生的，从而有效地形成了输入信号的立方形式。同样地，第四阶信号是通过在混合器 314 中对混合器 310 的输出求平方产生的。第五阶失真信号是通过在混合器 316 中将来自分离器 300 的输入信号混入混合器 314 的输出产生的。在混合器 318 中，来自混合器 310 的平方过的输入信号被混入来自混合器 314 的第四阶信号，以产生第六阶信号，第六阶信号随后在混合器 320 中被混入来自分离器 300 的输入信号以产生第七阶失真信号。

很显然对于专业人员而言，该方案能够扩展到所述任何阶生成的失真。而且还要注意，第二、第四和第六阶的失真信号能够分别从接头（tap）322、324 和 326 上提取，并且这些偶数阶的失真信号可以按预失真控制的形式来使用。

图 3 中的各种 DC 输入（DC1、DC2 等）用于通过注入适当的 DC 信号电平来从各种输出中消除所不希望的阶的失真，这里在考虑 DSP 实现的情况下，注入 DC 信号电平等效于固定数量的适当信号（+/-）的相加。而且还可以按照另外一种装置(mechanism)直接减去所不希望的信号来实现同样的目标。

这种预失真生成的方法的优点在于处理十分简单，其中每个混合器块（310、320 等）简单地相当于在多数 DSP 中仅包括单独指令循环的乘法。与某些传统形式的基带预失真生成不同，预失真生成装置直接在 300 提供的输入上进行运算，因此不需要存储器来存储系数，而这些传统形式的基带预失真生成中存储器需求较大，或者如果减少存储器需求，就必须执行实时内插计算，从而增加了处理功率的需求。

在图 1 的实施例中，可能需要高速模拟－数字转换器来取样 IF 频带反馈信号。图 4 中的实施例通过使用 DSP 外部的相关处理器作为简单地减少模拟－数字转换器的所需的取样频率的方法，避免了使用源漏极（resource-draining）快速模拟－数字转换器。在每个到同相和正交信道预失真器（相关器 410 和 412）的反馈路径中仅示出了单个相关器（混合器），但是正如后面参照图 5 所要描述的，该原理可以扩展到许多个相关器以及许多阶的失真。在其它方面，图 4 的实施例与图 1 的实施例相似。

本技术通过在频率偏移上变频成 IF 频带和数字－模拟转换（416、418）之后，将有关的基带失真分量（例如，第三阶）的形式与来自放大器输出的下变频（在 414 中）的反馈信号相关来运行的。控制信号在最小化放大器输出中的残余失真时，用于最小化该相关结果。当上变频失真分量时使用小的频率偏移保证了所希望的 IF 频带相关器的结果处于适当（音频）的频率上，因此消除了任何有关在相关器输出上的 DC 偏移的问题。音频频率相关结果随后可以由低取样频率转换器（420、422）来取样，并在 DSP 内被检测，这样消除了 DC 漂移的可能性。

应当理解，尽管此方法使用了高取样频率数字－模拟转换器（416、418）来提供偏移基带失真输出，但是该解决方法将占用比在图 1 的实施例中向 DSP

提供反馈信号时使用的高取样频率模拟－数字转换器更低的成本和更低的功率消耗（即使考虑到低取样频率模拟－数字转换器 420、422 的额外成本和功率消耗）。数字－模拟转换器 416 和 418 所需的动态范围（比特位数）还将大大小于在图 1 实施例的反馈路径的模拟－数字转换器中所需的动态范围。这样导致了进一步节省成本和功率。

现在将参照图 5 解释这些相关处理和展开成多个失真阶的操作。在该图所示的实施例中，I 和 Q 信道数字输入提供给数字信号处理器 500，处理器 500 包括分别在 I 和 Q 信道输入上进行运算的两个独立的预失真器 510 和 512。预失真器 510 和 512 分别如参照图 2 和 3 所述组成的。上变频器 514 对 I 和 Q 预失真的信号进行上变频以提供 IF 频带信号，IF 频带信号然后通过数字－模拟转换器 516 传输到电路的模拟部分。除了 I 和 Q 反馈路径在输送相关处理的分离器 518 和 520 中终止之外，系统的模拟部分以图 1 的实施例所述的相同方式运行。

控制处理是单独地对 I 和 Q 信道进行的，因而提供了独立的放大器特性的正交多项式模型。因为对于预失真器 510 和 512 中的每个预失真器而言控制方法基本上是相同的，所以现在将仅说明在正交信道数字输入信号上执行的预失真器 512 的控制方法。

在预失真器 512 中产生的奇数阶的失真 522、524、526、528 中的每个失真提供给各自的混合器 530、532、534、536 的输入，这些混合器的另一个输入提供有来自发生器 538 的正交移位的、偏移本地振荡器信号。应当理解，正交分离器 540 将偏移本地振荡器信号的相应的同相形式提供给用于预失真器 510 的控制装置。返回到预失真器 512 的控制装置，混合器 530、532、534、536 的输出表示了在预失真器 512 内产生的由偏移本地振荡器信号上变频的各个阶的失真。这些信号转换成模拟信号并提供给混合器 542、544、546、548 的输入。这些混合器使偏移上变频的失真阶数与提供给分离器 520 的反馈信号相关。

结果的音频范围信号由一组模拟－数字转换器取样并提供给 DSP 内的另外一组相关混合器 550、552、554、556。从在 560 中偏移本地振荡器 538 的输出与来自本地振荡器 558（在上变频器 514 中）的信号的相关结果中提取的信号提供给这些混合器中的每个混合器的另一个输入。LO 558 和 538 分别具有频率 70MHz 和 70.001MHz，混合器 560 的输出是 1KHz 的偏移频率。

接着对相关器 550、552、554、556 的输出进行积分以提供用于预失真器 512 的幅值调整元件的控制信号（已参照图 2 进行了说明）。同样的，由积分器产生的控制信号能够用于控制预失真器 512 的相位调整元件。以这种方式，完成了预失真器 510 和 512 的反馈控制。因为数字化地出现了积分和向前的相关，所以消除了任何降低失真（相互调制）电平的 DC 漂移或偏移的可能性。为了使处理保持一致，对于 DSP 时钟和 RF 本地振荡器而言有必要从相同的来源提取，或者以某种方式相位锁定。实现此的最简单的方法是从相同的晶体参照振荡器中即提取 DSP 时钟又提取本地振荡器。

应当注意，系统能够采用极坐标（幅值和相位）的形式执行，以替代前述的笛卡尔（I 和 Q）的形式。

在预失真器中可以包括自适应滤波以产生相对于生成的每一阶的失真的频率特性的任意幅值和/或相位。这能够对否则要经过不平衡相互调制失真的输出信号进行线性化。如图 6 所示，基本的预失真方法，如图 2 所述，能够通过在产生不同阶的失真的路径中的每个路径中包含自适应滤波器 610 等来进行改装。这些滤波器能够数字化地实现，并能够是递归或非递归类型，而且可以利用来自 RF 功率放大器的输出的反馈信号进行改进。基本系统还可以改进成在上变频和放大之前使用注入到主信号路径的导频信号。导频音调应当在 DSP 内产生（例如，使用数值控制的振荡器）并在 I 和 Q 输入信号的上变频之前叠加到 IF 频带。导频信号将在上变频和放大处理的适当期间完全经过来自输入信号的交叉调制失真，并且这种交叉调制失真能够从 RF 功率放大器的输出反馈以控制预失真器，如 UK 专利申请 9814391.0 所述。干扰导频信号的交叉调制分量能够利用反馈控制装置进行最小化，由于相互调制处理该控制装置依次使主信号的相关失真最小化。

说 明 书 附 图

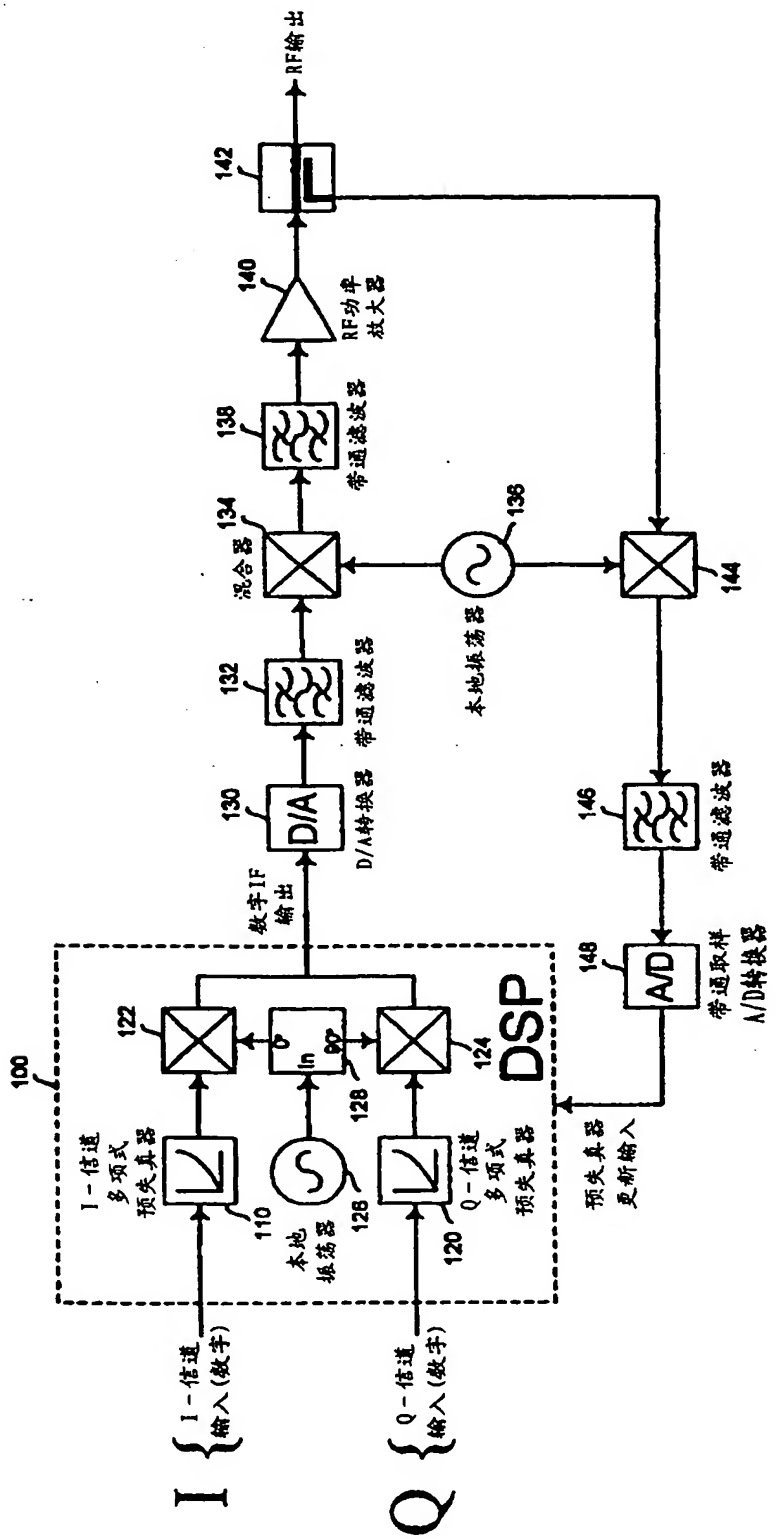

RF输出
142
140
RF功率放大器
138
带通滤波器
134
混合器
136
本地振荡器
144
132
带通滤波器
130
D/A
D/A转换器
数字IF输出
146
带通滤波器
148
A/D
带通取样A/D转换器
100
DSP
122
124
128
I
Q
I-信道多项式预失真器
110
本地振荡器
128
Q-信道多项式预失真器
120
预失真器更新输入
I-信道输入(数字)
Q-信道输入(数字)

图 1

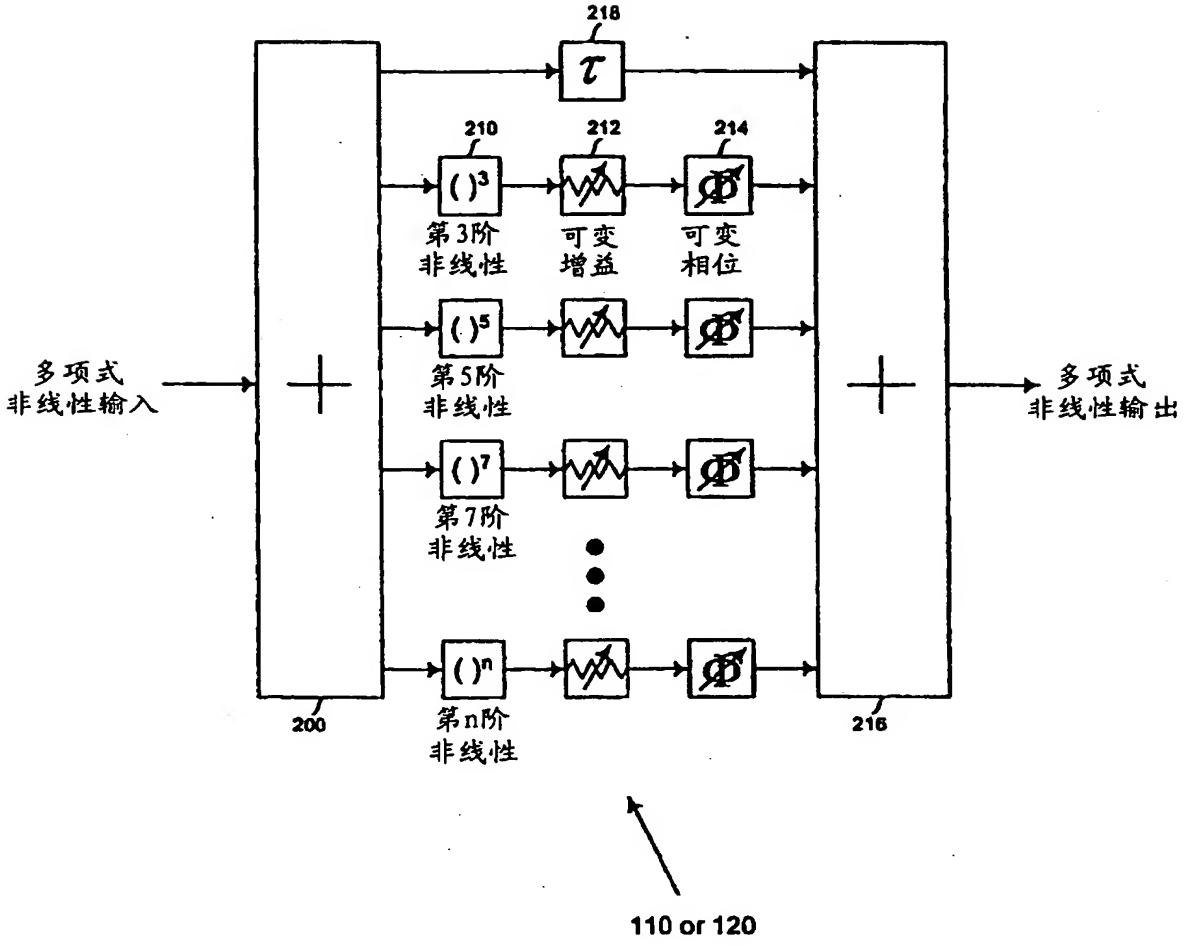

218
τ
210
212
214
( )3
第3阶
非线性
可变
增益
可变
相位
( )5
第5阶
非线性
多项式
非线性输入
多项式
非线性输出
( )7
第7阶
非线性
( )n
第n阶
非线性
200
216
110 or 120

图 2

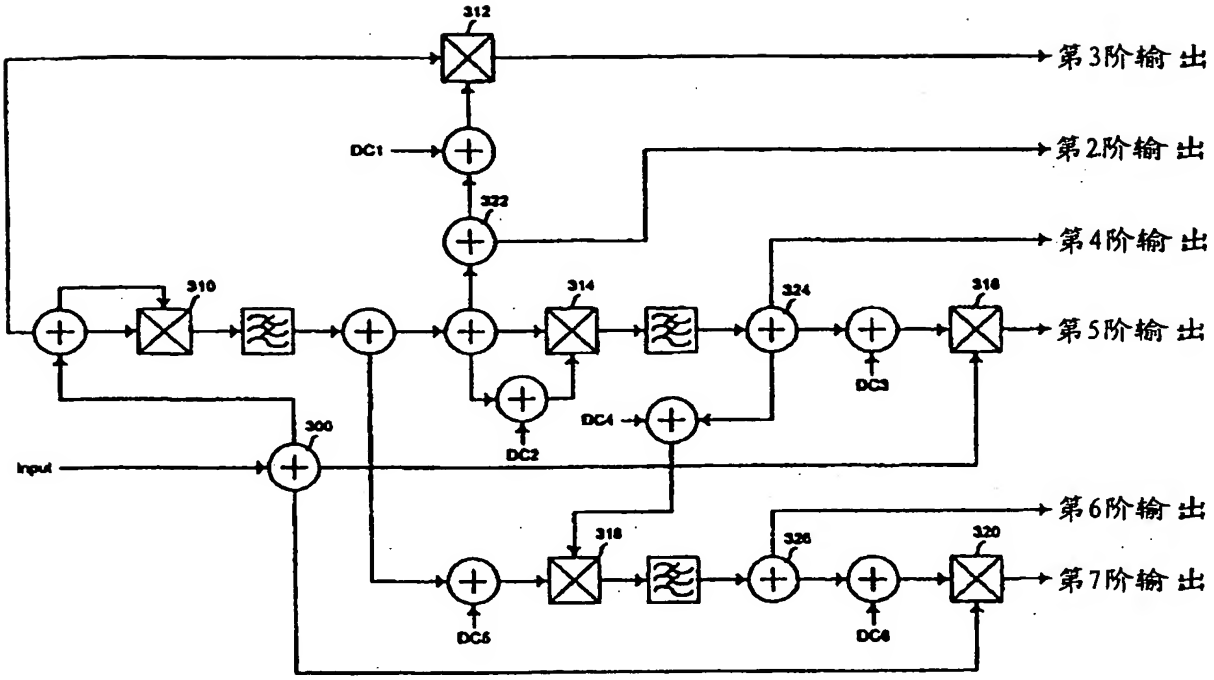

312
第3阶输出
DC1
第2阶输出
322
第4阶输出
310
314
324
316
第5阶输出
DC3
DC2
DC4
300
Input
第6阶输出
318
326
320
第7阶输出
DC5
DC6

图 3

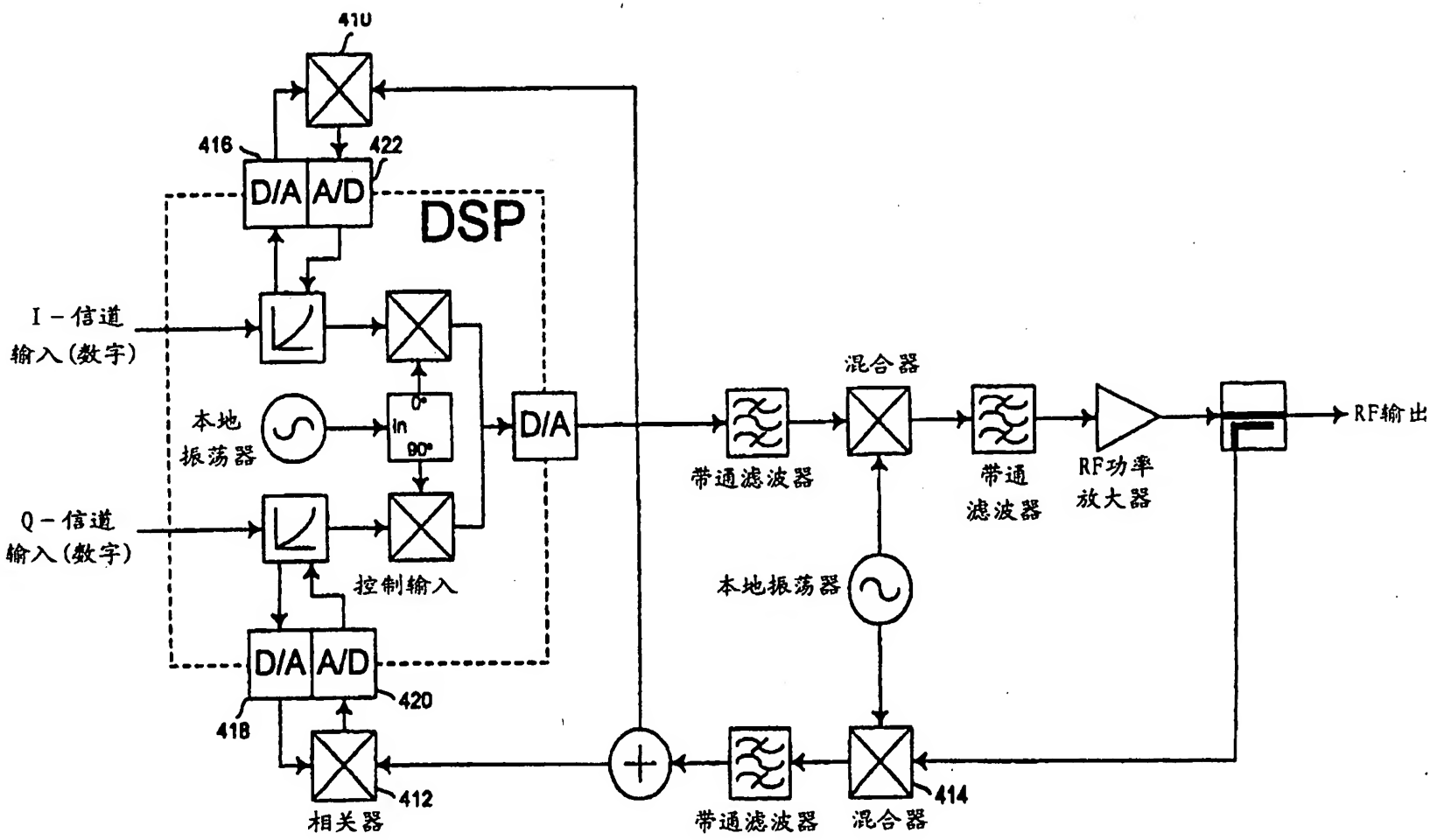

410
416
422
D/A
A/D
DSP
I－信道
输入(数字)
本地
振荡器
0°
in
90°
D/A
Q－信道
输入(数字)
控制输入
D/A
A/D
420
418
412
相关器
带通滤波器
混合器
带通
滤波器
RF功率
放大器
RF输出
本地振荡器
带通滤波器
混合器
414

图 4

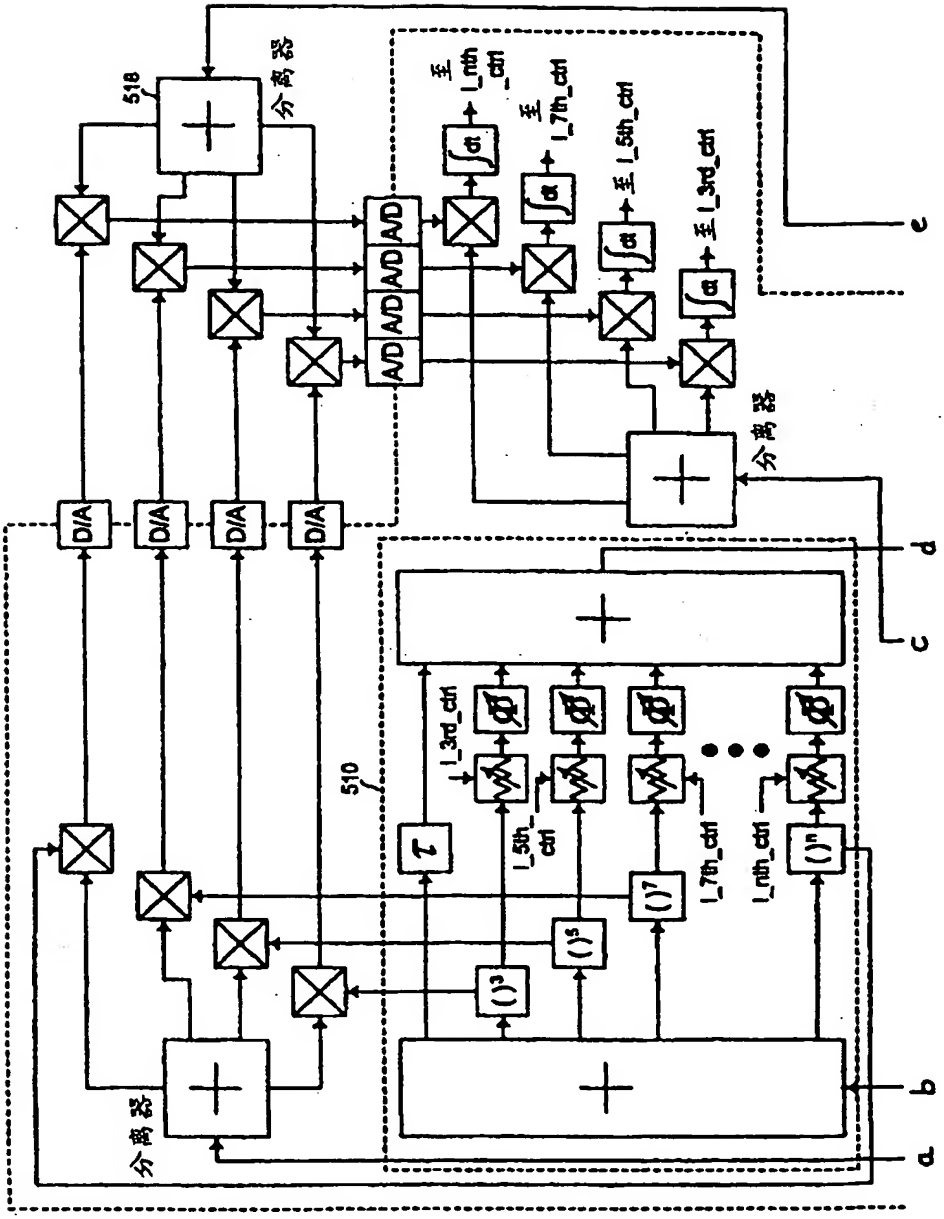

518
分离器
至 I_1st_ctrl
至 I_7th_ctrl
至 I_5th_ctrl
至 I_3rd_ctrl
A/D
A/D
A/D
A/D
e
D/A
D/A
D/A
D/A
d
c
510
I_3rd_ctrl
I_5th_ctrl
I_7th_ctrl
I_1th_ctrl
分离器
b
d

图 5a

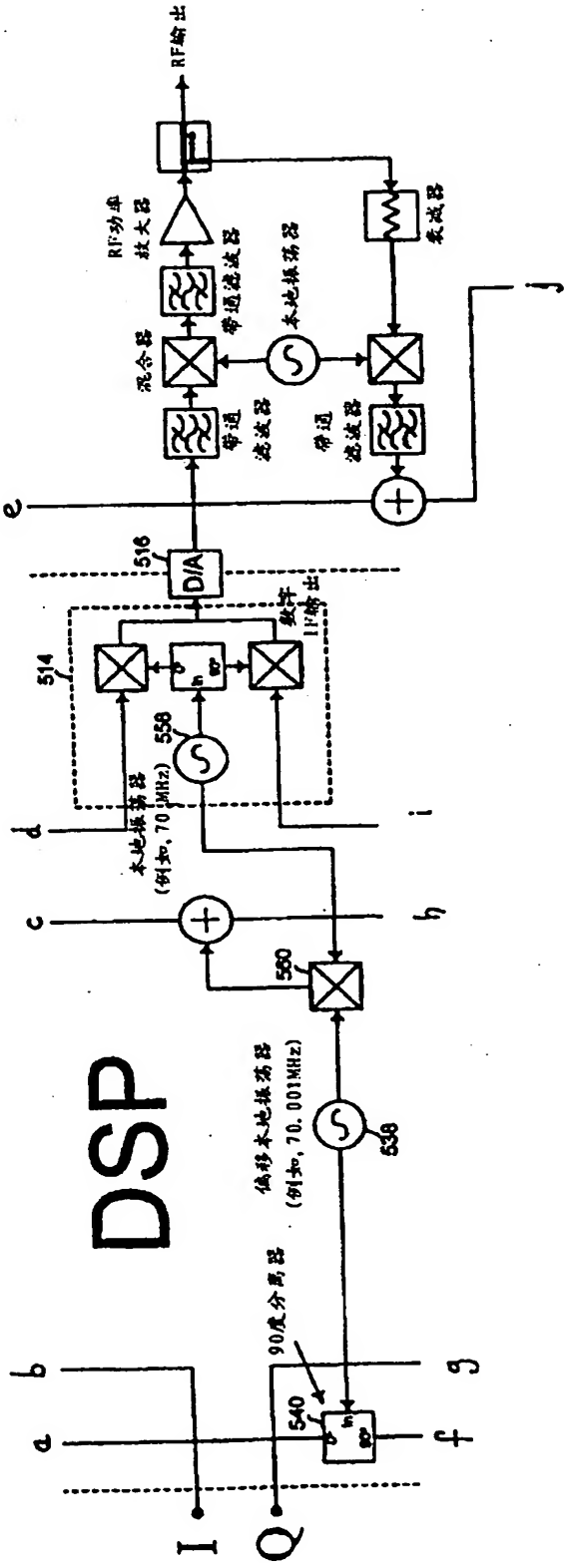

DSP
I
Q
a
b
c
d
e
f
g
h
i
j
90度分离器
540
偏移本地振荡器
(例如, 70.001MHz)
538
560
本地振荡器
(例如, 70.1MHz)
558
514
数字IF输出
516
D/A
带通滤波器
混合器
本地振荡器
带通滤波器
RF功率放大器
带通滤波器
RF输出
衰减器

图 5b

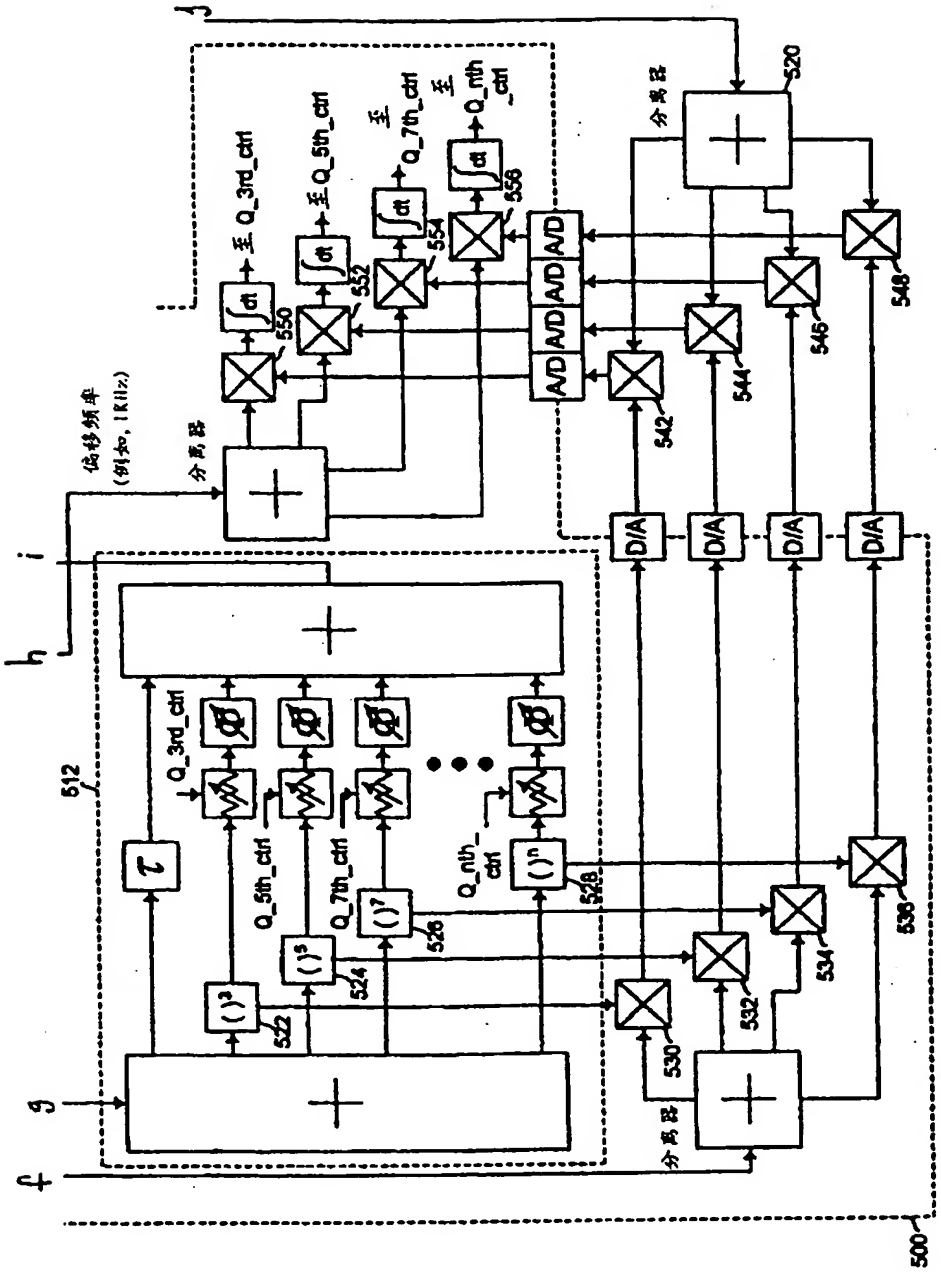

偏移频率
(例如，1KHz)
分离器
至 Q_3rd_ctrl
至 Q_5th_ctrl
至 Q_7th_ctrl
至 Q_nth_ctrl
A/D
D/A
Q_3rd_ctrl
Q_5th_ctrl
Q_7th_ctrl
Q_nth_ctrl
τ
512
500

图 5c

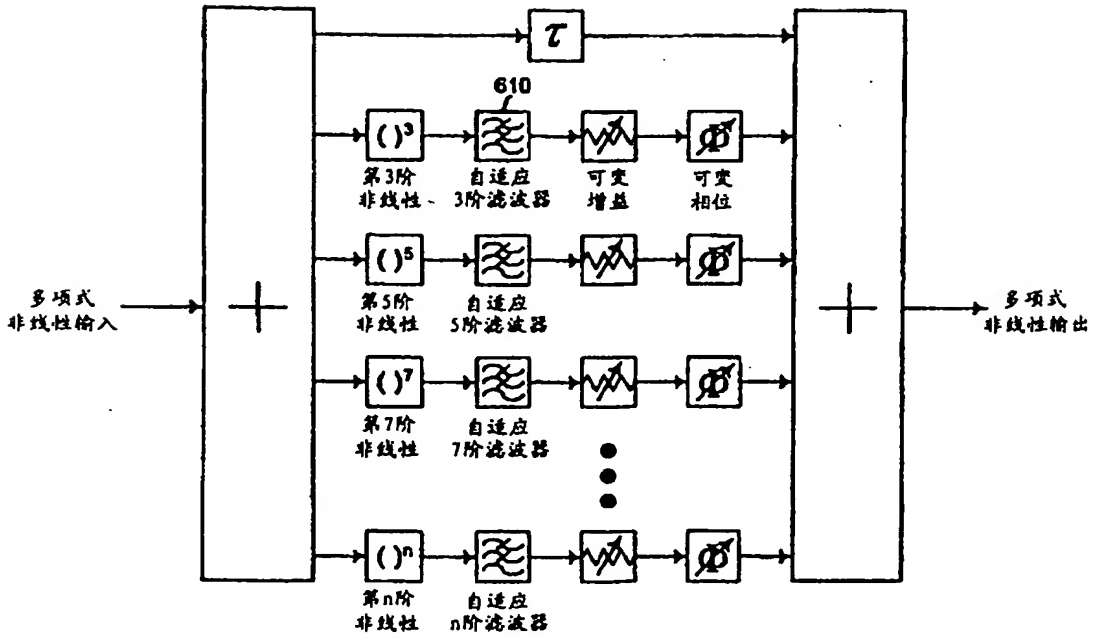

τ
610
( )³
第3阶
非线性
自适应
3阶滤波器
可变
增益
可变
相位
多项式
非线性输入
( )⁵
第5阶
非线性
自适应
5阶滤波器
( )⁷
第7阶
非线性
自适应
7阶滤波器
( )ⁿ
第n阶
非线性
自适应
n阶滤波器
多项式
非线性输出

图 6